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(54) **Eeprom system with bit error detecting function.**

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Description

The present invention relates to a non-volatile semiconductor programmable ROM with a bit error detector included therein.

An EEPROM is a non-volatile memory capable of electrical erasing and writing of information therein, and has found in recent years extensive application. For example, an IC card includes therein an EEPROM IC in the form of a chip for use in storage of important data (deposit information and health information etc.) by a user. The EEPROM is therefore required for a function of detecting any bit error involved in data in order to correctly store such informations. To detect any bit error caused in the EEPROM, it is well known to add a parity bit to bits constituting a word. For example, Nikkei Electronics (September 26, 1983) describes a principle for detection and correction of bit errors in "A high speed 1M bit mask ROM including therein an ECC circuit for improvement of the yield". Means to detect any error in data and indicate its position will here be described with reference to this reference.

Fig. 2 is a prior EEPROM system having an error detecting circuit which includes memory cells each for storage of 1 word-4 bits data. The EEPROM system comprises data memory cells 10 for storing data D0 to D3, data read circuit 30 for reading the data D0 to D3 stored in the data memory cells 10, bit lines 11 connecting between the data memory cells 10 and parts of the read circuits 30 respectively, logical output lines 12 connected with the read circuits 30 respectively for outputting the data read by the read circuits 30, parity memory cells 20 for storing parity bits, parity bit lines 21 connected between the parity memory cells 20 and the remaining parts of the read circuits 30, a bit error detecting circuit 2 composed of exclusive OR gates EOR1 to EOR3 each connected with the read circuits 30 via the logical output lines 12, and a position indicating circuit 1 composed of AND gates AND1 to AND4 connected with the exclusive OR gates EOR1 to EOR3 via logical output lines 22 for outputting error bit-indicating outputs e0 to e3, the AND gates AND1 to AND4 including therein parity data Po to P2. The EEPROM system is adapted to provide the three parity memory cells 20 correspondingly to the four memory cells 10 for each word, and further provide the parity memory cells 20 which store respectively pieces of parity informaton that form respectively even parities between the bit lines 21 and lines perpendicular thereto (word lines in general). Here, for example, the parity bit Po has an even parity relation with the data D0, D2, and D3, the parity bit P1 also an even parity relation with the data D2, D1, and D3, and the parity bit P2 further also an even parity relation with the data D0, D1, and D2. The bit error detecting circuit 2, i.e., the exclusive OR gates EOR1 to EOR3 respectively output a logical signal "0" when the even parity condition holds, and otherwise output a logical signal "1". For example, the exclusive OR gate EOR2 has the input bit lines D0, D1, and D3. Assumed here that D0 = "0", D1 = "0", D2 = "1", D3 = "0", P0 = "1", P1 = 0", and P2 = "1", the EOR2 outputs "0", satisfying the even parity condition. This assures no error. Provided now the data D1 is assumed to have an error bit "1" at a bit position where it should have a bit "0" originally, the EOR2 outputs "1" as a result of its logic and the EOR3 outputs too "1", causing the AND2 in the error position indicating cirucit 1 to output "1". This shows that the data D1 has any bit error therein. The prior EEPROM system with the error detecting circuit shown in Fig. 2 required three parity bits upon the data bits constituting 1 word being four, as described above.

On such a principle, (N + 1) parity memory cells is generally needed for 2^N memory cells which constitute 1 word, to detect bit errors and to indicate bits in error. Additionally, use of the even parity made impossible to detect even bit errors. In other words, it was impossible to detect completely a plurality of errors involved in 1 word. From these reasons described above, the prior EEPROM system with an error detecting circuit needed, upon fabrication thereof in 1 words-8 bits construction, a 4 bits memory cell for each word, resulting in the total bits being required to be more increased about 1.5 times than in that not including an error detecting circuit. The prior EEPROM systems thus suffered from a problem of a chip area being increased because of unsatisfactory chip efficiency to cause the cost-up of the device. It further suffered from another problem of incomplete error detection for a plurality of bits in principle.

In view of the drawbacks of the prior arts, it is an object of the present invention to provide an EEPROM system with an error detecting function capable of detection of any bit error and of indication of a position thereof in the data without the use of many parity memory cells each having insufficient chip efficiency.

Another object of the present invention is to provide an EEPROM system provided with an error detecting function capable of error correction for odd bits by additionally providing an 1 bit parity memory cell for each word.

Still another object of the present invention is to provide an EEPROM system provided with an error detecting function capable of detection of any memory cell which has the possibility of inadvantageously becoming deteriorated in the new future.

In accordance with the first aspect of the

present invention, an EEPROM system provided with an error detecting function comprises: a plurality of word lines; a plurality of sense lines; a plurality of MOS memory cells connected separately to the plurality of the word lines and to the plurality of the sense lines each for selecting one of the word lines and for storing data inputted therein through a selected one of said word lines; a plurality of bit lines connected separately to the MOS memory cells; a plurality of read circuits connected separately to the plurality of the bit lines for reading and outputting the data stored in the memory cells; and a plurality of intermediate state detecting circuits connected separately to the bit lines for detecting an intermediate state of each of the MOS memory cells other than writing and erasing states of the same and for outputting an error bit indicating signal.

Furthermore, in accordance with the second aspect of the present invention, an EEPROM system provided with an error detecting function comprises: a plurality of word lines; a plurality of sense lines; a plurality of MOS memory cells connected to the plurality of the word lines and to the plurality of the sense lines each for selecting one of the word lines and for storing data inputted therein through a selected one of said word lines; a parity check MOS memory cell for effecting parity check of 1 bit; a plurality of bit lines connected separately to the MOS memory cells and to the parity check MOS memory; a plurality of read circuits connected separately to the bit lines for reading and outputting the data stored in the memory cells; a plurality of intermediate state detecting circuits connected separately to the bit lines for detecting an intermediate state of each of the MOS memory cells other than writing and erasing states of the same and for outputting an error bit indicating signal, the intermediate state being a threshold potential between a threshold potential of the storage MOS memory cell in a writing state and a threshold potential of the storage MOS memory cell in a erasing state; and an additional intermediate state detecting circuit connected to the parity check MOS memory cell for detecting the intermediate state other than the writing and erasing states of the same and for outputting a parity check error bit indicating signal.

The objects, features and advantages of the present invention will become more apparent from the following description when taken in conjunction with the accompanying drawings in which preferred embodiments of the present invention are shown by way of illustrative example.

Fig. 1 is a circuit diagram illustrating a portion of an embodiment of an EEPROM system provided with an error detecting function according to the present invention;

Fig. 2 is a circuit diagram illustrating a portion of a prior EEPROM system provided with an error detecting function;

Fig. 3(a) is an equivalent circuit diagram of a memory cell for use in the EEPROM system of Fig. 1;

Fig. 3(b) is a view illustrating operating conditions of read, erase, and write for the EEPROM system of Fig. 1;

Fig. 4 is a view illustrating the characteristics of threshold voltage V_{TC} and sensitivity voltage Vs of a read circuit with respect to the number of reload of information in the memory cell of Fig. 1;

Fig. 5 is a view illustrating the change in the sensitivity voltage Vs of the read circuit;

Fig. 6 is a circuit diagram of an intermediate state detecting circuit of Fig. 1;

Fig. 7 is a circuit diagram illustrating a portion of a second embodiment of the EEPROM system provided with the error detecting function according to the present invention;

Fig. 8 is a circuit diagram illustrating a read circuit of Fig. 1; and

Fig. 9 is a circuit diagram illustrating an 1 bit correcting circuit.

In what follows, an embodiment of an EPROM system provided with an error detecting function will be described with reference to the accompanying drawings.

First, the arrangement and operation of a memory cell constituting the EEPROM system will be described with reference to Figs. 3, 4, and 5.

Fig. 3(a) is an equivalent circuit diagram of the memory cell for use in the EEPROM system, Fig. 3(b) is a view illustrating the operating conditions of read, erase, and write of the memory cell, Fig. 4 is a view illustrating the characteristics of threshold voltage V_{TC} of the memory cell and sensitivity voltage Vs of a read circuit both with respect to the number of times of write of information into the memory cell, and Fig. 5 is a view illustrating a change in the sensitivity voltage Vs of the read circuit.

The arrangement and operation of the memory cell is described for example in "16K bit EEPROM electrically erasable in a byte unit", Nikkei Electronics, No. June 23, 1980, pp 198 to 207.

Referring to Fig. 3(a), the memory cell includes a data selection MOS transistor Q1, and a storage memory MOS transistor Q2 for the type of double-layered polysilicon gate, both transistors being connected in series and the latter transistor having a floating gate 17.

The data selection MOS transistor Q1 has a first electrode coupled with a bit line 11 a second electrode coupled with the memory MOS transistor Q2, and a gate electrode coupled with a word line

15. While, the memory MOS transistor Q2 has a first electrode coupled with the second electrode of the data selection MOS transistor Q1, a gate electrode coupled with a sense (or program) line 16, the floating gate electrode 17, and a second electrode coupled with a ground line 13.

The storage MOS transistor Q2 forms a thin oxide film (tunneling oxide film) between the first electrode (drain) thereof and the floating gate 17, through which electrons and holes are injected into the floating gate 17 for erase and write operations.

Referring further to Fig. 3 (b), voltages at respective portions of the memory cell are assumed in read operation for example as follows: 2V on the bit line 11, 5V on the word line 15, 2V on the sense line 16, and ground potential on the ground line 13.

Here, accumulation of electrons on the floating gate 17 of the storage MOS transistor Q2 allows the threshold voltage V_{TC} for the storage MOS transistor Q2 to be raised. For this, the storage MOS transistor Q2 is turned off when the threshold voltage V_{TC} is above the potential of the sense line 16, while it being turned on when the V_{TC} is below the same potential.

Referring to the same figure, the voltages at the respective portions of the memory cell are assumed in the erase operation for example, as follows: 0V on the bit line 11, high voltage (e.g. 20V) on the word line 15, 20V on the sense line 16, and 0V on the ground line 13. The floating gate 17 of the storage MOS transistor Q2 is hereby injected with electrons through tunneling effect because of sufficiently high voltage being induced between the floating gate 17 and the first gate. This causes the threshold voltage V_{TC} of the storage MOS transistor Q2 to be raised.

Furthermore, referring to the same figure, the voltages at the respective portions of the memory cell are assumed in the write operation, for example, as follows: 20V on the bit line 11, 20V on the word line 15, 0V on the sense line 16, with the ground line kept at the floating state. The floating gate 17 is hereby forced to release therefrom the electrons accumulated thereon to a substrate and is instead injected thereinto with holes from the substrate . This causes the threshold voltage V_{TC} of the storage MOS transistor Q2 to be lowered.

Referring to Fig. 4, changes in the threshold voltage V_{TC} of the memory cell and in the sensitivity voltage Vs of a read circuit with respect to the number of times of reload operation for the memory cell will be described. In this situation conditions of applied voltage to and write time into the memory cell are kept unchanged. In the figures, a line L1 shows the threshold voltage V_{TV} (e.g., 1V) of the memory cell when no charge is accumulated on the floating gate 17 (neutral), with a line L2 showing the threshold voltage V_{TC} after the erase operation and a line L3 the same after the write operation. As illustrated in the figure, repeated reload operation produces trapping levels for electrons and holes in the tunneling oxide film, which causes deterioration of the characteristics of the memory cell such as reduction of the threshold voltage thereof, reduction of an interval to hold information therein, and lowering of dielectric voltage of gate insulating films involved, etc. Reload times of 10^3 causes no change in the threshold voltage V_{TC}, but those of 10^4 permit V_{TC} to start to be reduced.

In the memory cell having the characteristics shown by the lines L2, and L3 of Fig. 4, application of 2V to the sense line 16 upon the read operation causes a current to flow through the memory cell from the bit line. A read circuit (sense amplifier) described later senses and amplifies the current. In general, a large current flowing through the memory cell (this occurs in a write state) is outputted as a logic "0", while a small current (this occurs in an erase state) outputted as a logic "1". The sensitivity current (corresponding to the sensitivity voltage Vs of the sense line 16) of the read circuit (sense amplifier) is set typically larger than that flowing when the threshold voltage V_{TC} is applied to the gate of the storage MOS transistor Q2. As illustrated in Fig. 4, the sensitivity voltage Vs upon the threshold voltage V_{TC} being 1V (refer to the line L1) is 2V, and hence application of voltage 3V to the sense line 16 causes the sense amplifier (not shown) connected with the bit line 11 to invert its output logic. In the same fashion, with the threshold voltage V_{TC} along the line L2, the sensitivity voltage Vs is about 8V for example (refer to a line S2), and with the V_C along the line L3, the Vs is about -2V for example (refer to a line S3).

Here, a change in the threshold voltage V_{TC} of the memory cell having such characteristics will be described, the change being produced owing to insufficient dielectric voltage of the oxide film and a leak current through pin holes of the same.

As illustrated in Fig. 5, the sensitivity voltage Vs of the sense amplifier (not shown) is varied owing to the change in the threshold voltage of the MOS memory cell. In Fig. 5(a), when the memory cell in the write state is deteriorated to release completely charges accumulated thereon, the sensitivity voltage Vs is changed from -2V (refer to the line S2) to 2V (refer to the line S1). Additionally, in Fig. 5(b) when the memory cell in the erase state releases completely changes accumulated thereon, the sensitivity voltage Vs is changed from 8V (refer to the line S2) to 2V (refer to the line S1). The principle of the present invention is to utilize a fact that when the memory cell in the write or erase state releases parity charges accumulated thereon, the sensitivity voltage Vs does not cross a potential

of 2V for example as shown in Figs. 5(b) and (c).

An intermediate detecting circuit (bit error detecting circuit) according to the present invention is adapted to output an error signal as the MOS memory cell including therein any factor of faults or the possibility of becoming any complete fault state in near future, when the threshold voltage V_{TC} (or the sensitivity voltage V_S) lies in the vicinity of the intermediate level (e.g., line S_1) upon the read operation of the storage MOS transistor.

In the following, the embodiment of the EEPROM system including such an intermediate state detecting circuit (bit error detecting circuit) will be described with reference to Fig. 1. Fig. 1 illustrates part of the EEPROM system.

Referring to Fig. 1, the EEPROM system includes a memory matrix 10 composed of memory cells D0, D1, D2, and D3 for storing and outputting word information and of a plurality of bit lines 11, and a plurality of read circuits 30 connected to the respective bit lines 11. The EEPROM system further includes a plurality of the intermediate state detecting circuits 31 (bit error detecting circuits) connected to the respective bit lines 11 for outputting error bit indicating signals e_0, e_1, e_2, and e_3. Each of the memory cells D0, D1, D2, and D3 includes a selection MOS transistor Q1 and a storage MOS transistor Q2, as illustrated in Fig. 3(a) for example.

The read circuit 30 includes a CMOS inverter 301 and a PMOS transistor 302, as illustrated in Fig. 8.

The intermediate state detecting circuit 31 includes an NMOS transistor 43 composed of a gate electrode connected to one of the plurality of the bit lines 11, a first electrode, and a second electrode connected to a ground potential. The intermediate state detecting circuit 31 further includes a PMOS transistor 41 composed of a first electrode connected to a power supply V_{cc}, a second electrode, and a gate electrode, resistor means 42 connected to the second electrode of the PMOS transistor 41 and the first electrode of the NMOS transistor 43; MOS load means 40 connected between the power supply V_{cc} andthe gate electrodes of the PMOS transistor 41 and the NMOS transistor 43; and an AND gate 45 connected to, at one input thereof, the second electrode of the PMOS transistor 41 and connected, at the other input, to the first electrode of the NMOS transistor 43 via an inverter 44. The intermediate state detecting circuit 31 outputs a logic "0" when the memory cell is at the write and erase states (i.e., S_2 or S_3 in Fig. 4), while outputting a logic "1" when it is at the intermediate state (i.e., S_1, 1 to 4 V for example), as illustrated in Fig. 5. The NMOS transistor 43 inputs thereinto a signal from the bit line 11, and the AND gate 45 outputs an 1 bit error indicating signal corresponding to the associated bit line 11.

In succession, operation of the first embodiment will be described with reference to Figs. 1, 3, and 6.

Referring to Fig. 1, the first embodiment of the EEPROM system with an error detecting function of the present invention is shown. In Fig. 1, the read circuit 30 is set, as the sensitivity voltage V_s, to the read potential S_1 (e.g., 2 V) where no charge is accumulated on the floating gate of the memory cell 10. The intermediate state detecting circuit 31 is set, as the threshold level, to the intermediate potential (e.g., 1 to 4 V). The intermediate state detecting circuit 31 hereby outputs a logic "1" when the bit lines 11 are at 1 to 4 volts, while outputting a logic "0" when they are above 4 V (erasing state) or below 1 V (writing state).

Referring to Fig. 6, the intermediate state detecting circuit 31 is shown. As illustrated in the figure, the intermediate state detecting circuit 31 allows, when the bit line 11 is at 1 to 4 V, the AND gate 45 to output a logic "1" (error indicating signal) because the P and N transistors 41, 43 are conductive. When the bit line 11 is less than 1 V or more than 4 V, the AND gate 45 outputs a logic "0".

Here, in the EEPROM system of Fig. 1, it is assumed that data "0110" is stored in the memory cells D0 to D3 in the memory cell matrix 10, and the memory cell is fault so that the bit lines 11 upon read operation are at the intermediate potential (e.g., the state of Fig. 5(b)). In this situation, the read circuits 30 output 1 word data "0110" as output data d_0 to d_3, while the intermediate state detecting circuits 31 outputting data "0100" as bit error indicating output data, thus informing us of a fact that the bit of the memory cell D_1 will be deteriorated (i.e., changed to an error bit in future). This assures not only the indication of the bit error as described above, but also the utilization of the bit error indicating signal for correction of the error produced in the 1 word data (4 bits). Also, when the intermediate potential on the bit line 11 is less than the sensitivity voltage of the read circuit as shown in Fig. 5(c), a bit error indicating signal is outputted alike.

In the following, a second embodiment of the EEPROM system with an error detecting function of the present invention will be described with reference to Fig. 7.

As illustrated in Fig. 7, the second embodiment includes, additionally to the first embodiment of Fig. 1, a parity memory cell provided in the memory cell matrix 10 for checking 1 bit parity, an additional read circuit 50 connected to the parity memory cell P, and an additional intermediate state detecting circuit 60 connected to the parity memory cell P.

With the arrangement described above, the bit signals d_0 to d_p and the error bit indicating outputs e_0 to e_3 on logical output lines 12 corresponding to the respective memory cells are inputted together with a parity bit error indicating signal e_p into a bit correcting circuit 52 for example illustrated in Fig. 9.

The bit correcting circuit 52 includes for example a parity checking circuit 66, a plurality of EOR gates 58, and a plurality of AND gates 54, for correcting any error bit.

The second embodiment of the EEPROM system of Fig. 7 assures in error detecting and indicating signal also when the threshold voltage of a fault memory cell is equal to the sensitivity voltage of the read circuit, and the threshold voltage of the memory cell is changed from a high potential a predetermined intermediate level or less or from a low potential to the intermediate level or more. For example, when the memory cell D1 becomes an error state with its threshold value becoming the intermediate level (equal to or less than the sense level of the read circuit as shown in Fig. 5(d) for example), the read circuits d_0 to d_4 output read data "00100" including a parity bit. The parity check circuit 60, since the parity bit output is "0", effects the parity check and outputs a logic "1" if there are odd "1s", informing us of a fact that any bit of the read data involves an error. The position of the error bit can be identified because of the error bit indicating output is "01000" and hence the memory D1 is erroneous. Thereupon, the bit correcting circuit 60 inverts the output from the read circuit d_1 and outputs "01100" as a correct word.

Hereupon, correct data of the parity check may be set in a register (not shown) for use as corrected data. Thereupon, addition of an 1 parity bit to the data enables, differing from the prior arts, an error of the memory cell at the states of Fig. 5(a) and (b) to be detected irrespective of the number of bits constituting 1 word. The parity bit error signal e_p shown in Fig. 7 is employed as a control signal for the bit correcting circuit.

According to the present invention, as described above, bit line potentials are detected upon reading the EEPROM system, and an error signal is outputted provided those potentials are at the intermediate state. This requires less parity bits for detection and correction of any error, differing from the prior arts where many parity bits should be added. That is, the first embodiment of Fig. 1 requires no parity bit for correction of data, together with error detection for a plurality of bits. Additionally, the second embodiment of Fig. 7 can effect error correction with use of 1 bit parity for 1 word also from a state where charges are completely released. This sharply reduces a chip area of an EEPROM provided with an error detecting function, the reduction amounting to 33 % compared with a typical prior system.

Although certain preferred embodiments have been shown and described, it should be understood that many changes an modifications may be made therein without departing from the scope of the appended claims.

Claims

1. An EEPROM system with an error detecting function, comprising:
   (a) a plurality of word lines (15);
   (b) a plurality of sense lines (16);
   (c) a plurality of MOS memory cells (D0 through D3) connected separately to said word lines (15) and said sense lines (16);
   (d) a plurality of bit lines (11) connected separately to said MOS memory cells (D0 through D3);
   (e) a plurality of read circuits (30) connected separately to said plurality of the bit lines (11) for reading and outputting said data stored in said MOS memory cells (D0 through D3);
   characterised by
   (f) a plurality of intermediate state detecting circuits (31) connected separately to said bit lines (11) each for detecting an intermediate state (INTERMEDIATE LEVEL REGION) of one of said MOS memory cells (D0 through D3) other than writing and erasing states of the same and for outputting an error bit indicating signal,

2. An EEPROM system with an error detecting function according to Claim 1, wherein said intermediate state is a threshold voltage between a threshold voltage of each of said MOS memory cells (D0 through D3) in a writing state and a threshold voltage each of said MOS memory cells (D0 through D3) in a erasing state.

3. An EPROM system with an error detecting function according to Claim 1, wherein said MOS memory cell (D0 through D3) comprises a selection MOS transistor (Q1) and a storage MOS transistor (Q2), said selection MOS transistor (Q1) comprising a first electrode connected to the bit line (11), a gate electrode connected to the word line (15), and a second electrode, said storage MOS transistor (Q2) comprising a first electrode connected to said second electrode of said selection MOS transistor (Q1), a second electrode connected to a ground line, and a gate electrode connected to the sense line (16).

4. An EPROM system with an error detecting function according to Claim 1, wherein said intermediate state detecting circuit (31) comprises:

(a) an NMOS transistor (43) composed of a gate electrode connected to one of the plurality of said bit lines (11), a first electrode, and a second electrode connected to a ground potential;

(b) a PMOS transistor (41) composed of a first electrode connected to a power supply, a second electrode, and a gate electrode;

(c) resistor means (42) connected between said second electrode of said PMOS transistor (41) and said first electrode of said NMOS transistor (43);

(d) MOS load means (40) connected between said power supply and said gate electrodes of said PMOS transistor (41) and said NMOS transistor (43); and

(e) an AND gate (45) connected to, at one input thereof, said second electrode of said PMOS transistor (41) and connected, at the other input thereof, to said first electrode of said NMOS transistor (43) via an inverter (44) for inputting thereinto the voltage of said second electrode of said PMOS transistor (41) and the inverted voltage of that at said first electrode of said NMOS transistor (43) and for outputting said error indicating signal.

5. An EEPROM system with an error detecting function, comprising:

(a) a plurality of word lines (15);

(b) a plurality of sense lines (16);

(c) a plurality of memory cells (D0 through D3) connected to said plurality of the word lines (15) and to said plurality of the sense lines (16) each for selecting one of said word lines (15) and storing data inputted therein through a selected one of said word lines (15);

(d) a parity check MOS memory cell (P) for adding an 1 parity bit to the associated data;

(e) a plurality of bit lines (11) connected separately to said MOS memory cells (D0 through D3) and to said parity check MOS memory (P);

(f) a plurality of read circuits (30) separately connected to said bit lines (11) for reading and outputting said data stored in said memory cells (D0 through D3, P);

characterised by

(g) a plurality of intermediate state detecting circuits (31) connected separately to said bit lines (11) for detecting an intermediate state of said MOS memory cells (D0 through D3) other than write and erase states of the same and for outputting an error bit indicating signal; said intermediate state being a threshold voltage between a threshold voltage of each of said MOS memory cells (Q2) in a writing state and a threshold voltage of each of said MOS memory cells (Q2) in an erasing state; and

(h) an additional intermediate state detecting circuit connected to said parity check MOS memory cell (P) for detecting said intermediate state other than the writing and erasing states of each of said MOS memory cells (D0 through D3) and for outputting a parity check error bit indicating signal.

6. An EEPROM system with an error detecting function according to Claim 5, wherein said memory cell (D0 through D3, P) comprises a selection MOS transistor (Q1) and a storage MOS transistor (Q2) both connected in series, said selection MOS transistor (Q1) including a first electrode connected to the bit line (11), a gate electrode connected to the word line (15), and a second electrode, said storage MOS transistor (Q2) including a first electrode connected to the second electrode of said selection MOS transistor (Q1), a gate electrode connected to the sense line (16), and a second electrode connected to a ground line (13).

7. An EEPROM system with an error detecting function according to Claim 5, wherein said intermediate state detecting circuit (31, 60) comprises:

(a) an NMOS transistor (43) composed of a gate electrode connected to one of said bit lines (11), a first electrode, and a second electrode connected to the ground potential;

(b) a PMOS transistor (41) composed of a first electrode connected to a power supply, a second electrode, and a gate electrode;

(c) resistor means (42) connected to said second electrode of said PMOS transistor (41) and said first electrode of said NMOS transistor (43);

(d) MOS load means (40) connected between said power supply and said gate electrodes of said PMOS transistor (41) and of said NMOS transistor (43); and

(e) an AND gate (45) connected to, at one input thereof, said second electrode of said PMOS transistor (41) and connected to, at the other input thereof, said first electrode of said NMOS transistor (43) via an inverter (44) for inputting thereinto the voltage of said second electrode of said PMOS tran-

sistor (41) and the inverted voltage of that at said first electrode of said NMOS transistor (43) and outputting said error indicating signal.

Patentansprüche

1. Ein EEPROM-System mit Fehlererkennungsfunktion, das aufweist:
   (a) eine Vielzahl von Wortleitungen (15);
   (b) eine Vielzahl von Leseleitungen (16);
   (c) eine Vielzahl von MOS-Speicherzellen (D0 bis D3), die getrennt verbunden sind mit den Wortleitungen (15) und den Leseleitungen (16);
   (d) eine Vielzahl von Bitleitungen (11), die getrennt mit den MOS-Speicherzellen (D0 bis D3) verbunden sind;
   (e) eine Vielzahl von Leseschaltungen (30), die getrennt verbunden sind mit einer Vielzahl von Bitleitungen (11), zum Lesen und zur Ausgabe der in den MOS-Speicherzellen (D0 bis D3) gespeicherten Daten;
   gekennzeichnet durch:
   (f) eine Vielzahl von Zwischenstatus-Feststellschaltungen (31), die getrennt verbunden sind mit den Bitleitungen (11), jeweils zur Feststellung eines, vom Schreib- und Löschstatus unterschiedlichen Zwischenstatus (Zwischenpegelbereich) von einem der MOS-Speicherzellen und zur Ausgabe eines das Fehlerbit anzeigenden Signals.

2. Ein EEPROM-System mit Fehlererkennungsfunktion nach Anspruch 1, in welchem der Zwischenstatus eine Schwellwertspannung zwischen der Schwellwertspannung von jeder der MOS-Speicherzellen (D0 bis D3) im Schreibzustand und der Schwellwertspannung von jeder der MOS-Speicherzellen (D0 bis D3) im Löschzustand ist.

3. Ein EEPROM-System mit Fehlererkennungsfunktion nach Anspruch 1, in welchem die MOS-Speicherzelle (D0 bis D3) einen MOS-Auswahltransistor (Q1) und einen MOS-Speichertransistor (Q2) aufweist, wobei der MOS-Auswahltransistor (Q1) eine erste, mit der Bitleitung (11) verbundene Elektrode, eine mit der Wortleitung (15) verbundene Gate-Elektrode und eine zweite Elektrode aufweist, und wobei der MOS-Speichertransistor (Q2) eine erste, mit der Zweiten Elektrode des MOS-Auswahltransistors (Q1) verbundene Elektrode, eine zweite, mit einer Erdleitung verbundene Elektrode und eine mit der Leseleitung (16) verbundene Gate-Elektrode aufweist.

4. Ein EEPROM-System mit Fehlererkennungsfunktion nach Anspruch 1, in welchem die Zwischenstatus-Feststellschaltung (31) aufweist:
   (a) einen NMOS-Transistor (43), bestehend aus einer mit einer der Vielzahl von Bitleitungen (11) verbundenen Gate-Elektrode, einer ersten Elektrode und einer zweiten, mit einem Erdpotential verbundenen Elektrode;
   (b) einen PMOS-Transistor (41), bestehend aus einer ersten, mit einer Netzversorgung verbundenen Elektrode, einer zweiten Elektrode und einer Gate-Elektrode;
   (c) eine Widerstandseinrichtung (42), die zwischen die zweite Elektrode des PMOS-Transistors (41) und die erste Elektrode des NMOS-Transistors (43) geschaltet ist;
   (d) eine MOS-Ladeeinrichtung (40), die zwischen die Netzversorgung und die Gate-Elektroden des PMOS-Transistors (41) und des NMOS-Transistors (43) geschaltet ist; und
   (e) ein UND-Glied (45), dessen einer Eingang mit der zweiten Elektrode des PMOS-Transistors (41) und dessen anderer Eingang über einen Inverter (44) mit der ersten Elektrode des NMOS-Transistors (43) verbunden ist, zur Eingabe der Spannung an der zweiten Elektrode des PMOS-Transistors (41) und der invertierten Spannung derjenigen an der ersten Elektrode des NMOS-Transistors (43) und zur Ausgabe des Fehleranzeigesignals.

5. Ein EEPROM-System mit Fehlererkennungsfunktion, das aufweist:
   (a) eine Vielzahl von Wortleitungen (15);
   (b) eine Vielzahl von Leseleitungen (16);
   (c) eine Vielzahl von Speicherzellen (D0 bis D3), die mit der Vielzahl der Wortleitungen (15) und der Vielzahl der Leseleitungen (16) verbunden sind, jeweils zur Auswahl einer der Wortleitungen (15) und zum Speichern der Daten, die durch eine aus den Wortleitungen (15) Ausgewählte eingegeben wurde;
   (d) eine Paritätsprüf-MOS-Speicherzelle (P) zum Hinzufügen eines 1-Paritätsbits zu den zugeordneten Daten;
   (e) eine Vielzahl von Bitleitungen (11), die getrennt mit den MOS-Speicherzellen (D0 bis D3) und dem Paritätsprüf-MOS-Speicher (P) verbunden sind;
   (f) eine Vielzahl von Leseleitungen (30), die getrennt mit den Bitleitungen (11) verbunden sind, zum Lesen und zur Ausgabe der in den Speicherzellen (D0 bis D3, P) ge-

speicherten Daten;
gekennzeichnet durch:

(g) eine Vielzahl von Zwischenstatus-Feststellschaltungen (31), die getrennt mit den Bitleitungen (11) verbunden sind, zur Feststellung eines, vom Schreib- und Löschstatus unterschiedlichen Zwischenstatus der MOS-Speicherzellen (D0 bis D3) und zur Ausgabe eines das Fehlerbit anzeigenden Signals; wobei der Zwischenstatus eine Schnellwertspannung zwischen der Schnellwertspannung von jeder der MOS-Speicherzellen (Q2) im Schreibzustand und der Schnellwertspannung von jeder der MOS-Speicherzellen (Q1) im Löschzustand ist; und

(h) eine zusätzliche Zwischenstatus-Feststellschaltung, die mit der Paritätsprüf-MOS-Speicherzelle (P) verbunden ist, zur Feststellung des vom Schreib- und Löschstatus unterschiedlichen Zwischenstatus von jeder der MOS-Speicherzellen (D0 bis D3) und zur Ausgabe eines das Paritätsprüf-Fehlerbit anzeigenden Signals.

6. Ein EEPROM-System mit Fehlererkennungsfunktion nach Anspruch 5, in welchem die Speicherzelle (D0 bis D3,P) einen MOS-Auswahltransistor (Q1) und einen MOS-Speichertransistor (Q2) aufweist, die in Reihe geschaltet sind, wobei der MOS-Auswahltransistor (Q1) eine erste, mit der Bitleitung (11) verbundene Elektrode, eine mit der Wortleitung (15) verbundene Gate-Elektrode und eine zweite Elektrode aufweist, und wobei der MOS-Speichertransistor (Q2) eine erste, mit der zweiten Elektrode des MOS-Auswahltransistors (Q1) verbundene Elektrode, eine mit der Leseleitung (16) verbundene Gate-Elektrode und eine zweite, mit einer Erdleitung (13) verbundene Elektrode aufweist.

7. Ein EEPROM-System mit Fehlererkennungsfunktion nach Anspruch 5, in welchem die Zwischenstatus-Feststellschaltung (31, 60) aufweist:

(a) einen NMOS-Transistor (43), bestehend aus einer mit einer der Bitleitungen (11) verbundenen Gate-Elektrode, einer ersten Elektrode und einer zweiten, mit dem Erdpotential verbundenen Elektrode;

(b) einen PMOS-Transistor (41), bestehend aus einer ersten, mit der Netzversorgung verbundenen Elektrode, einer zweiten Elektrode und einer Gate-Elektrode;

(c) einer Widerstandseinrichtung (42), die mit der zweiten Elektrode des PMOS-Transistors (41) und der ersten Elektrode des NMOS-Transistors (43) verbunden ist;

(d) eine MOS-Ladeeinrichtung (40), die zwischen die Netzversorgung und die Gate-Elektroden des PMOS-Transistors (41) und des NMOS-Transistors (43) geschaltet ist; und

(e) ein UND-Glied (45), dessen einer Eingang mit der zweiten Elektrode des PMOS-Transistors (41) und dessen anderer Eingang über einen Inverter (44) mit der ersten Elektrode des NMOS-Transistors (43) verbunden ist, zur Eingabe der Spannung der zweiten Elektrode des PMOS-Transistors (41) und der invertierten Spannung derjenigen an der ersten Elektrode des NMOS-Transistors (43) und zur Ausgabe des Fehleranzeigesignals.

Revendications

1. Un système de mémoire morte programmable et effaçable par des moyens électriques, ou EEPROM, comportant une fonction de détection d'erreur, comprenant :

(a) un ensemble de lignes de mot (15);

(b) un ensemble de lignes de détection (16);

(c) un ensemble de cellules de mémoire MOS (D0 à D3), connectées séparément aux lignes de mot (15) et aux lignes de détection (16);

(d) un ensemble de lignes de bit (11) connectées séparément aux cellules de mémoire MOS (D0 à D3);

(e) un ensemble de circuits de lecture (30) connectés séparément à l'ensemble des lignes de bit (11), pour lire et présenter en sortie les données qui sont enregistrées dans les cellules de mémoire MOS (D0 à D3);

caractérisé par

(f) un ensemble de circuits de détection d'état intermédiaire (31), connectés séparément aux lignes de bit (11), chacun d'eux étant destiné à détecter un état intermédiaire (REGION DE NIVEAU INTERMEDIAIRE) de l'une des cellules de mémoire MOS (D0 à D3), autre que des états d'écriture et d'effacement de la cellule considérée, et à fournir en sortie un signal d'indication de bit erroné.

2. Un système de mémoire EEPROM comportant une fonction de détection d'erreur selon la revendication 1, dans lequel l'état intermédiaire est une tension de seuil entre une tension de seuil de chacune des cellules de mémoire MOS (D0 à D3) dans un état d'écriture, et une

tension de seuil de chacune des cellules de mémoire MOS (D0 à D3) dans un état d'effacement.

3. Un système de mémoire EEPROM comportant une fonction de détection d'erreur selon la revendication 1, dans lequel la cellule de mémoire MOS (D0 à D3) comprend un transistor MOS de sélection (Q1) et un transistor MOS de mémorisation (Q2), ce transistor MOS de sélection (Q1) comprenant une première électrode connectée à la ligne de bit (11), une électrode de grille connectée à la ligne de mot (15) et une seconde électrode, tandis que le transistor MOS de mémorisation (Q2) comprend une première électrode connectée à la seconde électrode du transistor MOS de sélection (Q1), une seconde électrode connectée à une ligne de masse, et une électrode de grille connectée à la ligne de détection (16).

4. Un système de mémoire EEPROM comportant une fonction de détection d'erreur selon la revendication 1, dans lequel le circuit de détection d'état intermédiaire (31) comprend :
(a) un transistor NMOS (43), constitué par une électrode de grille connectée à une ligne de l'ensemble de lignes de bit (11), une première électrode, et une seconde électrode connectée à un potentiel de masse;
(b) un transistor PMOS (41) constitué par une première électrode connectée à une alimentation, une seconde électrode et une électrode de grille;
(c) des moyens résistifs (42) connectés entre la seconde électrode du transistor PMOS (41) et la première électrode du transistor NMOS (43);
(d) des moyens de charge de type MOS (40) connectés entre l'alimentation et les électrodes de grille du transistor PMOS (41) et du transistor NMOS (43); et
(e) une porte ET (45) dont une entrée est connectée à la seconde électrode du transistor PMOS (41), et dont l'autre entrée est connectée à la première électrode du transistor NMOS (43), par l'intermédiaire d'un inverseur (44), pour appliquer à cette porte la tension de la seconde électrode du transistor PMOS (41) et la tension inversée par rapport à la tension présente sur la première électrode du second transistor NMOS (43), et pour fournir en sortie le signal d'indication d'erreur.

5. Un système de mémoire EEPROM comportant une fonction de détection d'erreur, comprenant :
(a) un ensemble de lignes de mot (15);
(b) un ensemble de lignes de détection (16);
(c) un ensemble de cellules de mémoire (D0 à D3) connectées à l'ensemble des lignes de mot (15) et à l'ensemble des lignes de détection (16), ayant chacune pour fonction de sélectionner l'une des lignes de mot (15) et de mémoriser des données reçues par l'intermédiaire de l'une sélectionnée des lignes de mot (15);
(d) une cellule de mémoire MOS de contrôle de parité (P), destinée à ajouter un bit de parité 1 aux données associées;
(e) un ensemble de lignes de bit (11) connectées séparément aux cellules de mémoire MOS (D0 à D3) et à la cellule de mémoire MOS de contrôle de parité (P);
(f) un ensemble de circuits de lecture (30) connectés séparément aux lignes de bit (11) pour lire et présenter en sortie les données qui sont enregistrées dans les cellules de mémoire (D0 à D3, P);
caractérisé par
(g) un ensemble de circuits de détection d'état intermédiaire (31), connectés séparément aux lignes de bit (11), pour détecter un état intermédiaire des cellules de mémoire MOS (D0 à D3), autre que des états d'écriture et d'effacement de ces cellules, et pour fournir en sortie un signal d'indication de bit erroné; cet état intermédiaire étant une tension de seuil entre une tension de seuil de chacune des cellules de mémoire MOS (Q2) dans un état d'écriture, et une tension de seuil de chacune des cellules de mémoire MOS (Q2) dans un état d'effacement; et
(h) un circuit de détection d'état intermédiaire supplémentaire, connecté à la cellule de mémoire MOS de contrôle de parité (P), pour détecter l'état intermédiaire autre que les états d'écriture et d'effacement de chacune des cellules de mémoire MOS (D0 à D3), et pour fournir en sortie un signal d'indication de bit erroné de contrôle de parité.

6. Un système de mémoire EEPROM comportant une fonction de détection d'erreur selon la revendication 5, dans lequel la cellule de mémoire (D0 à D3, P) comprend un transistor MOS de sélection (Q1) et un transistor MOS de mémorisation (Q2) qui sont connectés en série, le transistor MOS de sélection (Q1) comprenant une première électrode qui est connectée à la ligne de bit (11), une électrode de grille qui est connectée à la ligne de mot

(15), et une seconde électrode, tandis que le transistor MOS de mémorisation (Q2) comprend une première électrode connectée à la seconde électrode du transistor MOS de sélection (Q1), une électrode de grille connectée à la ligne de détection (16), et une seconde électrode connectée à une ligne de masse (13).

7. Un système de mémoire EEPROM comportant une fonction de détection d'erreur selon la revendication 5, dans lequel le circuit de détection d'état intermédiaire (31, 60) comprend :
   (a) un transistor NMOS (43) comprenant une électrode de grille connectée à l'une des lignes de bit (11), une première électrode et une seconde électrode connectée au potentiel de masse;
   (b) un transistor PMOS (41) comprenant une première électrode connectée à une alimentation, une seconde électrode et une électrode de grille;
   (c) des moyens résistifs (42) connectés à la seconde électrode du transistor PMOS (41) et à la première électrode du transistor NMOS (43);
   (d) des moyens de charge de type MOS (40) connectés entre l'alimentation et les électrodes de grille du transistor PMOS (41) et du transistor NMOS (43); et
   (e) une porte ET (45) dont une entrée est connectée à la seconde électrode du transistor PMOS (41) et dont l'autre entrée est connectée à la première électrode du transistor NMOS (43) par l'intermédiaire d'un inverseur (44), pour appliquer à cette porte la tension de la seconde électrode du transistor PMOS (41) et la tension inversée par rapport à celle présente sur la première électrode du transistor NMOS (43), et pour fournir en sortie le signal d'indication d'erreur.

Fig. 1

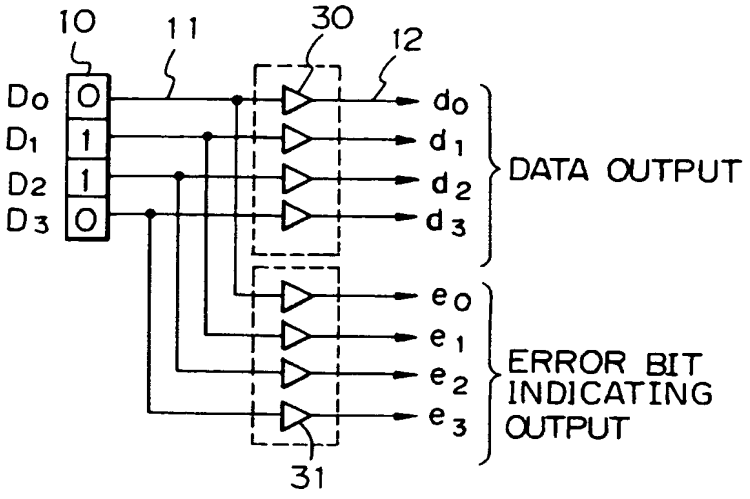

10
11
30
12
Do
D1
D2
D3
0
1
1
0
do
d1
d2
d3
DATA OUTPUT
eo
e1
e2
e3
ERROR BIT INDICATING OUTPUT
31

Fig. 4

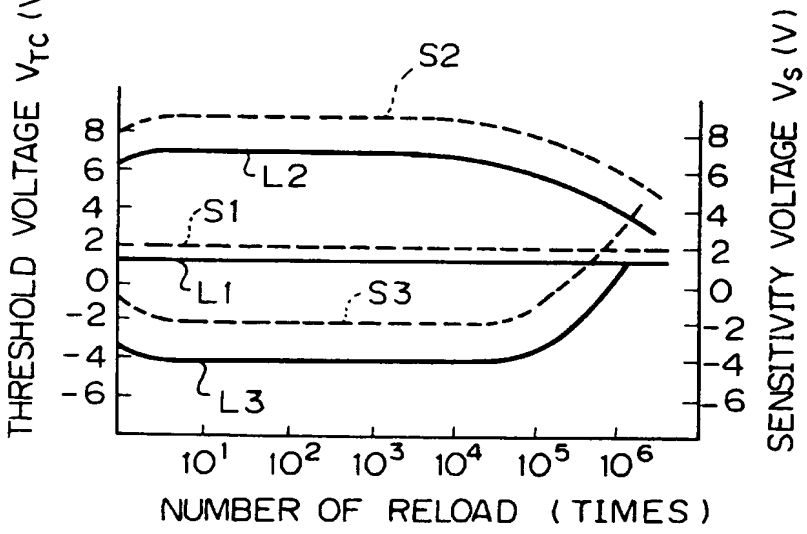

THRESHOLD VOLTAGE V_{TC} (V)
SENSITIVITY VOLTAGE V_S (V)
S2
L2
S1
L1
S3
L3
8
6
4
2
0
-2
-4
-6
10^1 10^2 10^3 10^4 10^5 10^6
NUMBER OF RELOAD (TIMES)

Fig. 2

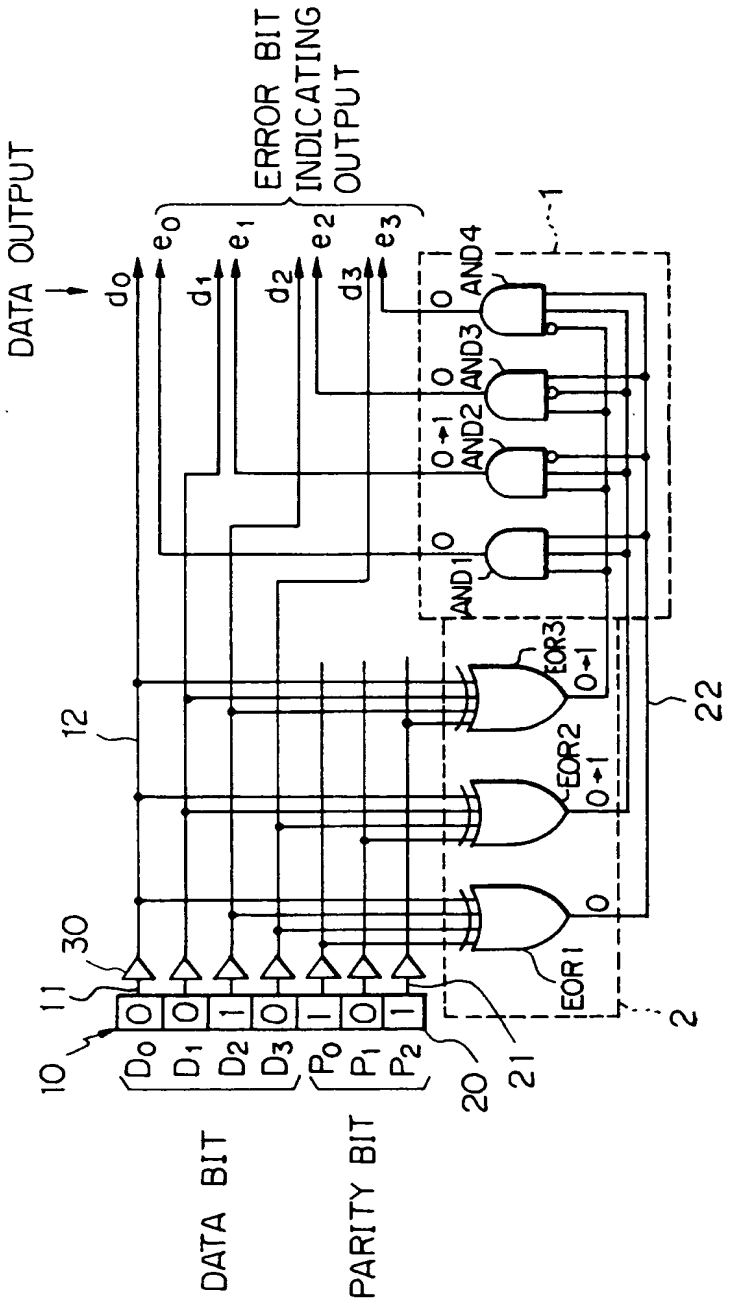
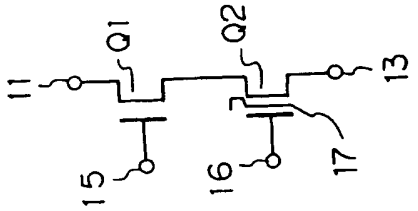

DATA OUTPUT
ERROR BIT INDICATING OUTPUT
d_0
d_1
d_2
d_3
e_0
e_1
e_2
e_3
AND4
AND3
AND2
AND1
EOR3
EOR2
EOR1
0→1
12
22
30
11
10
20
21
2
1
D_0 D_1 D_2 D_3 P_0 P_1 P_2
DATA BIT
PARITY BIT

Fig. 3

OPERATION MODE	VOLTAGE AT EACH PORTION			
	BIT LINE	WORD LINE	SENSE LINE	GROUND LINE
IN READING	2 v	5 v	2 v	0 v
IN ERASING	0 v	20 v	20 v	0 v
IN WRITING	20 v	20 v	0 v	FLOATING

(b)



(a)

Fig. 5

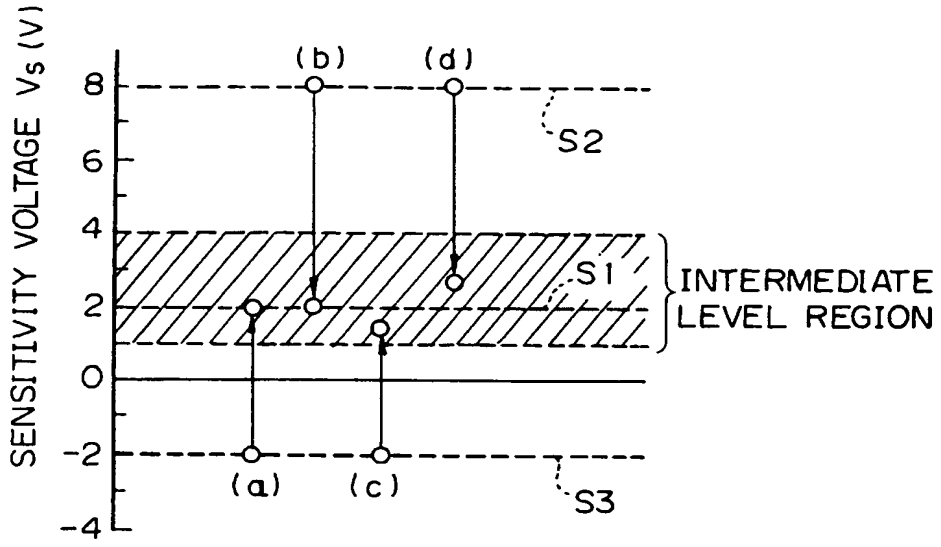

SENSITIVITY VOLTAGE Vs (V)
8
6
4
2
0
-2
-4
(b)
(d)
(a)
(c)
S1
S2
S3
INTERMEDIATE LEVEL REGION

Fig. 6

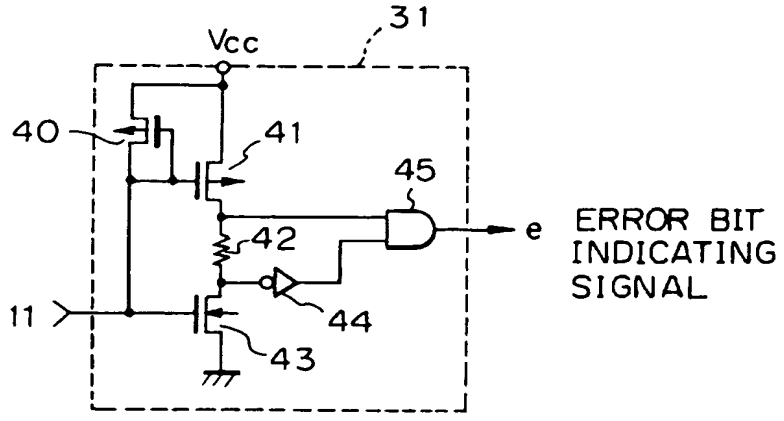

Vcc
31
40
41
45
42
e
ERROR BIT INDICATING SIGNAL
11
44
43

Fig. 7

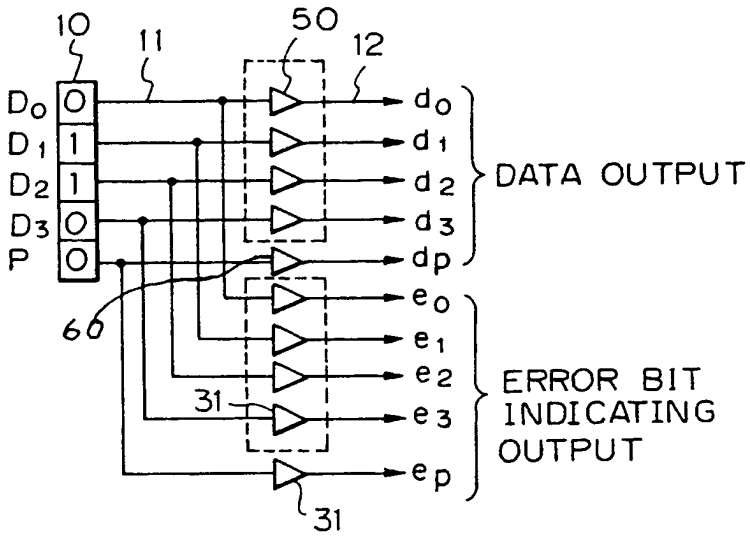
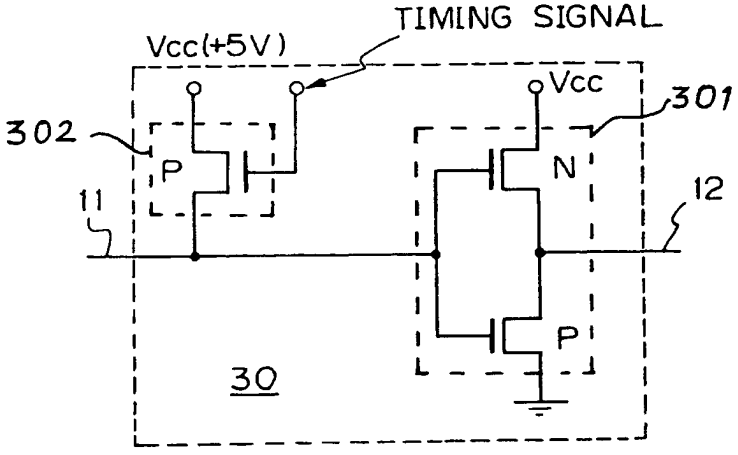

10
11
50
12
D0
D1
D2
D3
P
0
1
1
0
0
d0
d1
d2
d3
dp
DATA OUTPUT
e0
e1
e2
e3
ep
ERROR BIT INDICATING OUTPUT
60
31
31

Fig. 8


TIMING SIGNAL
Vcc(+5V)
Vcc
301
302
P
N
11
12
P
30

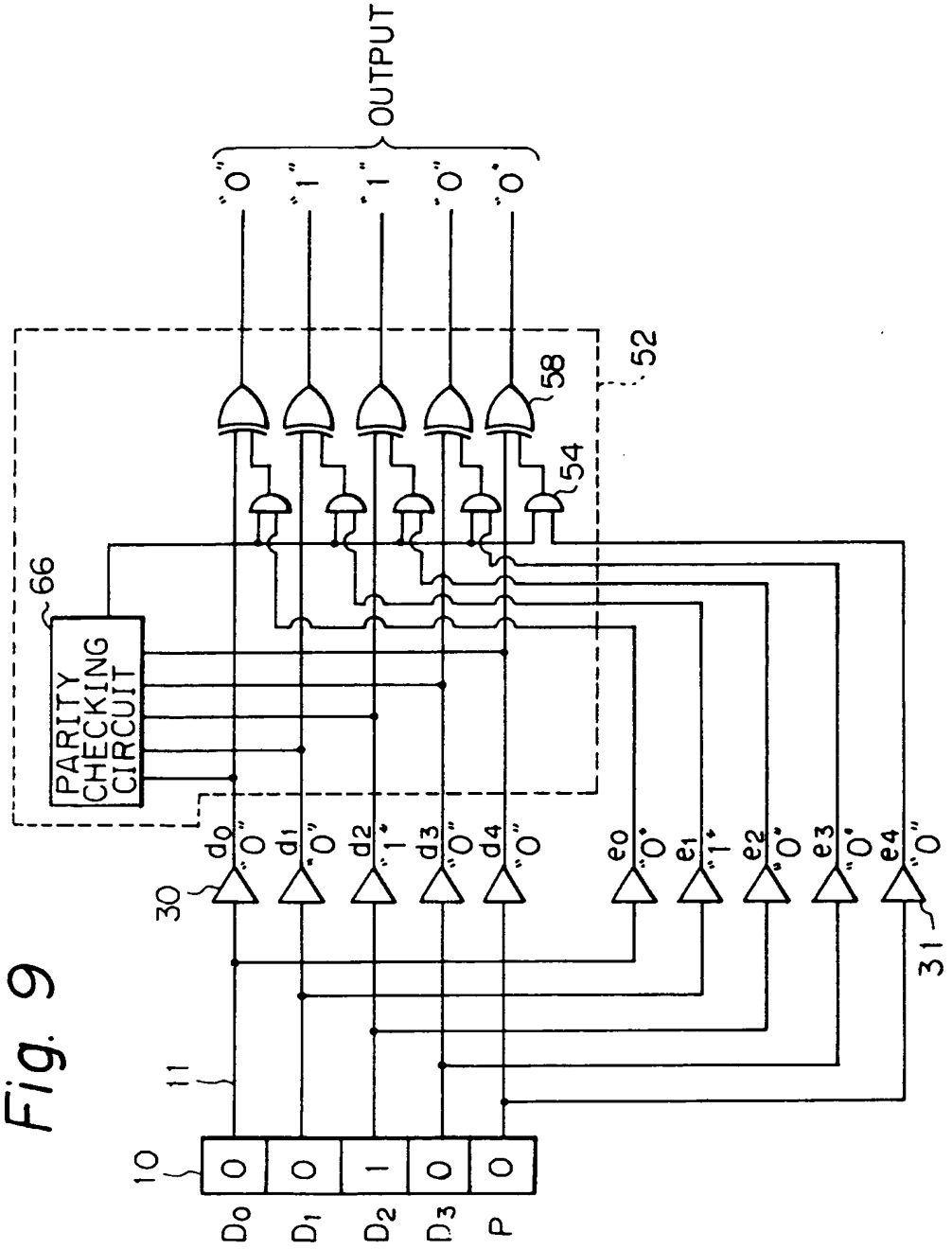

OUTPUT
"0"
"1"
"1"
"0"
"0"
52
58
54
66
PARITY CHECKING CIRCUIT
d0 "0"
d1 "0"
d2 "1"
d3 "0"
d4 "0"
e0 "0"
e1 "1"
e2 "0"
e3 "0"
e4 "0"
30
31
11
10
0 0 1 0 0
D0 D1 D2 D3 P

Fig. 9